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ScienceDirect
Applied Surface Science 253 (2007) 3595–3599
applied surface science
www.elsevier.com/locate/apsusc

High-density-plasma (HDP)-CVD oxide to thermal oxide wafer bonding for strained silicon layer transfer applications

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Received 29 May 2006; received in revised form 23 July 2006; accepted 24 July 2006
Available online 14 September 2006

Abstract

Direct wafer bonding between high-density-plasma chemical vapour deposited (HDP-CVD) oxide and thermal oxide (TO) has been investigated. HDP-CVD oxides, about 230 nm in thickness, were deposited on Si(0 0 1) control wafers and the wafers of interest that contain a thin strained silicon (sSi) layer on a so-called virtual substrate that is composed of relaxed SiGe (~4 μm thick) on Si(0 0 1) wafers. The surfaces of the as-deposited HDP-CVD oxides on the Si control wafers were smooth with a root-mean-square (RMS) roughness of <1 nm, which is sufficiently smooth for direct wafer bonding. The surfaces of the sSi/SiGe/Si(0 0 1) substrates show an RMS roughness of >2 nm. After HDP-CVD oxide deposition on the sSi/SiGe/Si substrates, the RMS roughness of the oxide surfaces was also found to be the same, i.e., >2 nm. To use these wafers for direct bonding the RMS roughness had to be reduced below 1 nm, which was carried out using a chemo-mechanical polishing (CMP) step. After bonding the HDP-CVD oxides to thermally oxidized handle wafers, the bonded interfaces were mostly bubble- and void-free for the silicon control and the sSi/SiGe/Si(0 0 1) wafers. The bonded wafer pairs were then annealed at higher temperatures up to 800 °C and the bonded interfaces were still found to be almost bubble- and void-free. Thus, HDP-CVD oxide is quite suitable for direct wafer bonding and layer transfer of ultrathin sSi layers on oxidized Si wafers for the fabrication of novel sSOI substrates.
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Keywords: Direct wafer bonding; High-density-plasma-CVD oxide; Atomic force microscopy; Infra-red transmission imaging; Strained silicon on insulator; Bonded interface; Transmission electron microscopy

1. Introduction

Enhanced carrier mobilities in strained Si (sSi) leads to an improvement in the performance of nano-CMOS transistors fabricated using ultrathin sSi layers [1–5]. The sSi layers are grown on so-called virtual substrates which are comprised of strain-relaxed $Si_{1-x}Ge_x$ buffer layers grown on Si(0 0 1) substrates [3,6]. The ultrathin sSi layers grown on these virtual substrates can be transferred onto oxidized Si handle wafers using direct wafer bonding and layer transfer techniques leading to the formation of strained silicon-on-insulator (sSOI) substrates [4,7]. The sSOI substrates combine the benefits of enhanced carrier mobilities in sSi and lower parasitic capacitances in SOI substrates [2,3,5]. The fabrication of sSOI involves direct wafer bonding between sSi containing virtual substrates and Si handle wafers with the oxide layer deposited on the sSi layer, the Si handle wafer or both [7,8]. After the wafer bonding step, the sSi layers can be transferred from the virtual substrate onto the Si handle wafers either by grinding combined with selective wet chemical etching or by the hydrogen implantation-induced layer splitting of the virtual substrate parallel to the bonding interface and the selective wet chemical etching [4,7,8]. The successful transfer of uniform sSi layer over an entire 200 mm diameter wafer area to a large extent depends upon the quality of the bonded interface between the virtual substrate and the Si handle wafer. In some previous reports, it has been shown that for the wafer bonding purpose various intermediate oxides such as PECVD (plasma-enhanced chemical vapour deposition), LTO (low temperature oxide), tTo (thin thermal oxide), *etc*. could be utilized in order

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doi:10.1016/j.apsusc.2006.07.077

to achieve good interface quality and sufficiently high bonding energy [8–12].

In this report we have carried out a systematic investigation of the bonding behavior between a high-density-plasma chemical vapour deposition (HDP-CVD) oxide and a thermal oxide (TO). The HDP-CVD oxides are widely used for gap-fill purposes in shallow trench isolation (STI) and pre-metal dielectric (PMD) applications since they exhibit high aspect ratio deposition [13,14]. In the present investigation we deposited HDP-CVD oxide layers on sSi layers that resided on virtual substrates and on Si control wafers. These wafers were then bonded with thermally oxidized Si(0 0 1) handle wafers. The quality of the bonded interface after annealing the bonded wafer pairs at higher temperatures was assessed using infra-red transmission imaging and scanning acoustic microscopy.

2. Experimental

The HDP-CVD oxide layers were deposited on 200 mm diameter Si(0 0 1) control wafers as well as sSi layers on SiGe/Si(0 0 1) virtual substrates using AMAT Ultima HDP-CVD chamber originally dedicated for STI trench fill. The deposition was carried out at a pressure of <10 mTorr using SiH_4, O_2 and Ar gases without helium backside cooling. The gas flow rates were as follows: SiH_4—110 sccm, O_2—220 sccm and Ar—85 sccm. Power delivery by Standard Generator Rack used for HDP Chamber was: Top Gen.—1300 W/Side Gen.—3100 W/Bias Gen.—2600 W, and the frequency was: Top/Side—2 MHz, Bias—13.56 MHz. The thickness of the HDP-CVD oxide layers was about 230 nm in all cases. The root-mean-square (RMS) roughness of the oxide surfaces was measured by atomic force microscopy (AFM) using a Digital Instruments Dimension 3000 microscope operated in the tapping mode. In case of the HDP-CVD oxide deposited on sSi/SiGe/Si(0 0 1) substrates, chemo-mechanical polishing (CMP) of the oxide was carried out using a AMAT Mirra Mesa CMP tool to reduce the RMS roughness below 1 nm required for subsequent direct wafer bonding [15,16]. After the CMP step the thickness of the HDP-CVD oxide was reduced from 230 nm to about 90 nm. The wafer bonding was carried out between the HDP-CVD oxide and a thermal oxide on the Si(0 0 1) handle wafers of about 150 nm thickness using a Suss Microtec's CL200 cleaner. The quality of the bonded interface was assessed using infra-red (IR) transmission imaging and scanning acoustic microscopy (SAM). For SAM measurements, a Sonoscan C-SAM 300DX acoustic micro-imaging system was used. The bonded pairs were first annealed at 300 °C for 5 h and then at 500 °C for 2 h. For some Si control wafers with HDP-CVD oxide layers, an outgassing step at 850 °C for 1 h was carried out. The bonded pairs were then annealed up to 800 °C for 1 h. The microstructural characterization of the bonded interface was carried out by cross-sectional transmission electron microscopy (XTEM) using a Philips CM20T machine operated at a voltage of 200 kV.

3. Results and discussion

The thickness of the HDP-CVD oxide deposited on 200 mm Si(0 0 1) control wafers was about 230 nm as measured by spectroscopic ellipsometry using KLA UV1280 measurement system. The thickness was measured at nine different locations over the surface of the wafers with an edge exclusion of 3 mm. The maximum to minimum thickness variation over the whole wafer surface was about 12 nm. The surface of the as-deposited oxide on Si control wafers was found to be smooth and uniform with an RMS roughness of 0.25 nm on a 10 μm $\times$ 10 μm AFM scan area. In contrast, for PECVD oxides the RMS roughness in the as-deposited state is usually above 1 nm and hence a chemo-mechanical polishing (CMP) step is required to reduce the RMS roughness below 1 nm required for the wafer bonding [11,17]. The Si control wafer with HDP-CVD oxide was bonded to a thermally oxidized Si(0 0 1) handle wafer and the bonded interface quality was assessed with IR imaging technique. Fig. 1(a) shows the IR image of the bonded wafer pair. The bonded interface is found to be void- and bubble-free over the whole wafer area. The wafer pair was then annealed at 200 °C for 5 h and subsequently at 500 °C for 2 h. The IR image of the

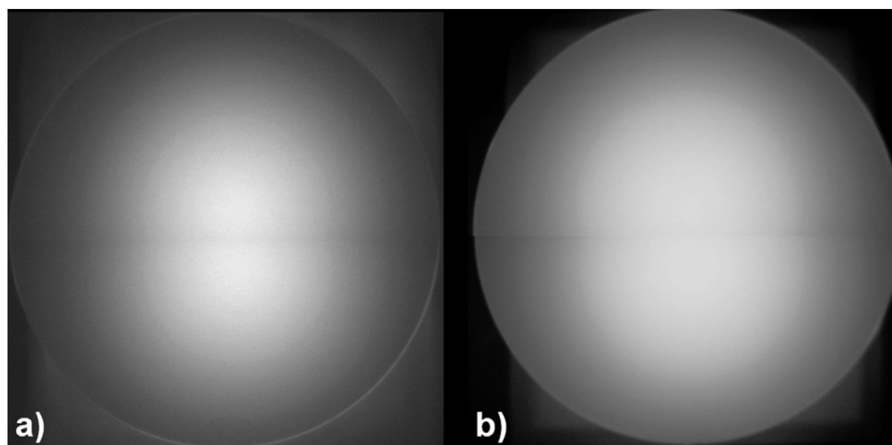

Fig. 1. Infra-red transmission image of HDP-CVD oxide to thermal oxide bonded wafer pair (a) without annealing and (b) after annealing first at 200 °C for 5 h and then at 500 °C for 2 h.

bonded interface after these annealing steps is shown in Fig. 1(b) and it is still found to be void- and bubble-free. But the IR transmission imaging can detect only the macroscopic voids or bubbles (having size of about 1 mm or greater) at the bonded interface. Hence we performed SAM measurements on the bonded pair to observe microscopic voids (having size of about a few tens of micrometers) at the bonded interface. The SAM measurements were performed at different locations on the 8-in. diameter bonded wafer pair. An SAM image of a section of the bonded wafer pair after annealing at 200 °C for 5 h and then at 500 °C for 2 h is shown in Fig. 2. This image shows the absence of any microscopic voids or bubbles at the bonded interface even after annealing of the bonded wafer pair. For layer transfer applications using hydrogen implantation-induced layer splitting and wafer bonding techniques, usually a two step annealing sequence for the bonded wafer pairs similar to that one reported here is carried out [7,9]. This suggests that the presented HDP-CVD oxide is suitable for the layer transfer applications in order to fabricate novel substrates such as sSOI. Apart from assessing the quality of the bonded interface, we measured the bonding energy of the HDP-CVD oxide to thermal oxide bonded wafer pair using crack-opening method [15]. The bonding energy after annealing at 200 °C for 5 h was found to be about 0.80 J/m^2, while the bonding energy after annealing first at 200 °C for 5 h and then at 500 °C for 2 h increased to a value of about 1.0 J/m^2.

The HDP-CVD oxide layers were also deposited on sSi/$Si_{0.78}Ge_{0.22}$/Si(0 0 1) substrates. Before the deposition of oxide layers the RMS roughness of the surface of the virtual substrate was measured by AFM and found to be about 1.8 nm. After the deposition of 230 nm thick oxide the RMS roughness remained the same. Thus a CMP step was needed prior to direct wafer bonding. After the CMP step the thickness of the oxide reduced to 90 nm with maximum to minimum variation on the whole wafer of about 20–40 nm. The RMS roughness of the surface was reduced down to 0.23 nm on an AFM scan area of 10 μm × 10 μm, well below 1 nm so that the wafers could be bonded (Fig. 3). Wafer bonding was carried out to a thermally oxidized Si(0 0 1) handle wafer. The IR transmission image of the bonded interface is shown in Fig. 4(a) and it can be seen that the interface is free of voids. The bonded wafer pair was then annealed sequentially at 200 °C for 5 h and 500 °C for 2 h. The IR image of the annealed bonded pair is shown in Fig. 4(b). A few small voids appeared after the annealing sequence but apart from them bonded interface is of good quality. These small voids may be related to some particulate impurities at the interface, which could not be removed completely during the RCA cleaning process of the oxides. It is expected that with a more careful cleaning process this problem can be easily alleviated. Additionally, the SAM measurements on the bonded pair after the above-mentioned annealing sequence showed the absence of any microscopic voids at the interface.

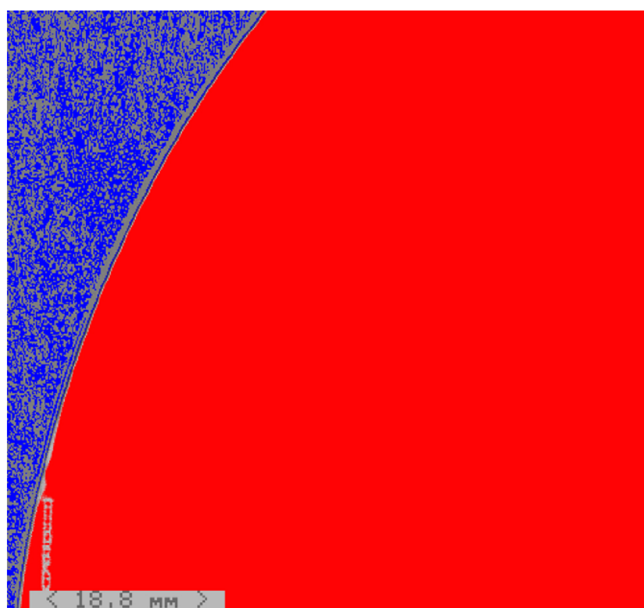

Fig. 2. Scanning acoustic microscopic image of the HDP-CVD oxide to thermal oxide bonded wafer pair after annealing first at 200 °C for 5 h and then at 500 °C for 2 h. The pixel size of the SAM image is 512 × 480. No microscopic voids or bubbles (having size of a few tens of micrometers) are observed at the bonded interface (note that the small unbonded area in the lower left corner of the image is due to laser scribing mark on one of the wafers).

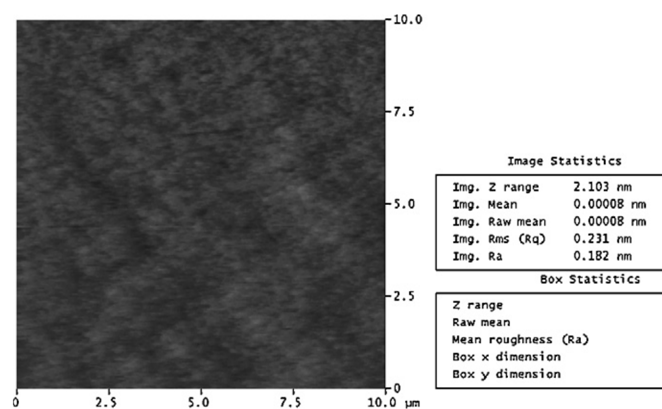

Fig. 3. AFM image of the surface of HDP-CVD oxide deposited on sSi/$Si_{0.78}Ge_{0.22}$/Si substrate after chemo-mechanical polishing (CMP). After CMP the thickness of HDP-CVD oxide is reduced from 230 to 90 nm.

To check the behavior of the bonding interface after annealing at temperatures higher than 500 °C, we carried out an outgassing step of the HDP-CVD oxide prior to bonding in argon ambient at 850 °C for 1 h using a slow ramping rate of 1 °C/min. When the outgassing was not performed before the bonding between HDP-CVD oxide and thermal oxide, a number of big voids or bubbles appeared at the interface after annealing the wafer pair at 800 °C for 1 h. But if an outgassing step was done prior to bonding, the bonded interface did not show any voids or bubbles when annealed up to 800 °C for 1 h as can be seen from Fig. 5. It is known that during the deposition of plasma CVD oxides, undesired by-products or gas molecules are incorporated into the deposited oxide film and result in outgassing during the subsequent thermal processing [10,11]. The outgassing of the gas molecules during high temperature annealing of the bonded wafer pair causes the formation of voids at the bonded interface. To avoid the formation of voids, it is required to carry out an outgassing step for the deposited plasma CVD oxides at a slightly higher temperature in inert gas

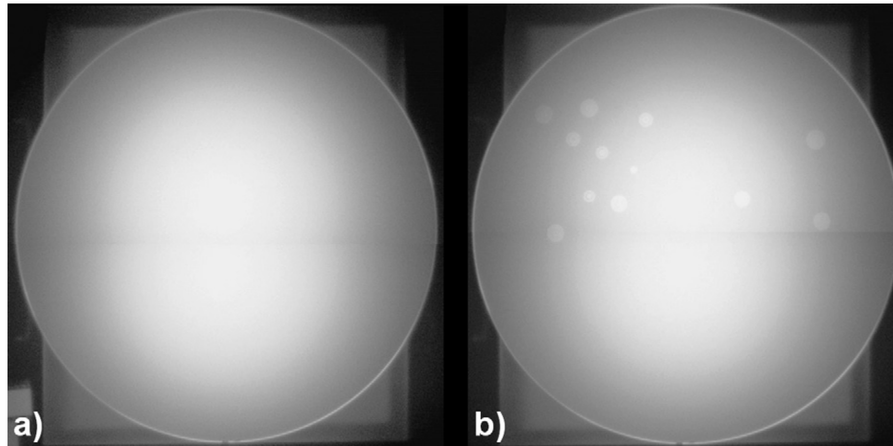

Fig. 4. Infra-red transmission image of HDP-CVD oxide (on sSi/SiGe/Si substrate) to thermal oxide bonded wafer pair (a) without annealing and (b) after annealing first at 200 °C for 5 h and then at 500 °C for 2 h.

ambient than the ultimate processing temperature in order to remove all the undesired gas molecules out of the CVD oxide. In the present case of HDP-CVD oxide, the substrate temperature during the deposition was on the order of 700 °C. Hence the HDP-CVD oxide to thermal oxide bonded wafer pair did not show any void formation at the bonded interface up to an annealing temperature of about 700 °C even without any outgassing step for the oxide film prior to bonding. But when the annealing temperature of the bonded pair was increased up to 800 °C, there were gas molecules which still persisted in the oxide film and started outgassing after a temperature of 700 °C resulting in the formation of interface voids. Hence it was required that prior to bonding, the HDP-CVD oxide be outgassed at 850 °C in inert gas ambient so that all the undesired gas molecules are removed from the oxide film. After this outgassing step, the bonded pair could be annealed up to 800 °C without the formation of any voids at the interface. Finally it is noteworthy that we performed XTEM measurements on the bonded interface in order to assess the quality of the interface at the nanoscopic scale. Fig. 6 shows the XTEM image of the bonded interface involving the HDP-CVD oxide deposited wafers annealed at 850 °C for 1 h prior to bonding. The interface between the HDP-CVD oxide and the thermal oxide is smooth and free of any nanoscopic voids. In some earlier reports involving Si/Si wafer bonding, it was shown that nanovoids appeared at the interface after annealing the bonded wafer pairs at higher temperatures [18,19]. But in the present case, we did not observe any nanovoids after annealing the bonded wafer pair up to 800 °C for 1 h. In the CMOS transistor fabrication process on sSi, the gate oxidation step utilizes temperatures of about 800 °C for less than 1 h [20]. Hence it is important that the bonded interface should not exhibit voids or bubbles during the processing of the transistors. In the present work it is clearly shown that if HDP-CVD oxide on sSi/SiGe/Si(0 0 1) wafers is used as an intermediate oxide for the layer transfer purpose to fabricate sSOI substrates, then prior to bonding an outgassing step at 850 °C for 1 h will be required to avoid the formation of voids or bubbles at the bonded interface during the CMOS fabrication process on sSOI wafers.

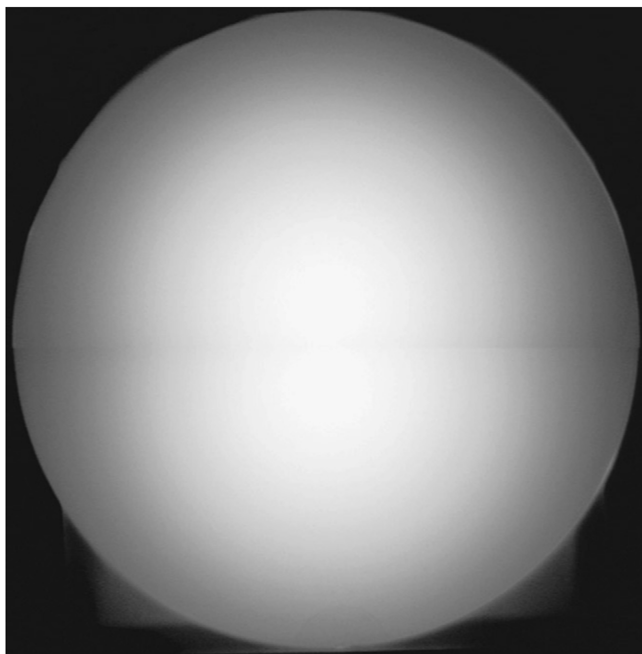

Fig. 5. Infra-red transmission image of HDP-CVD oxide to thermal oxide bonded wafer pair after annealing at 800 °C for 1 h. Before bonding the outgassing for the HDP-CVD oxide was carried out at 850 °C for 1 h.

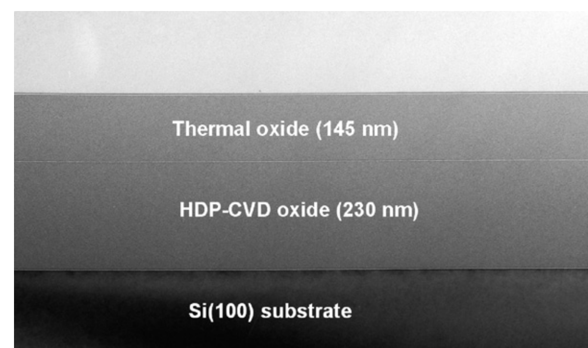

Fig. 6. XTEM image of the HDP-CVD oxide to thermal oxide bonded interface after annealing at 800 °C for 1 h.

4. Conclusions

HDP-CVD oxide layers were deposited on 200 mm diameter Si(0 0 1) control and sSi/SiGe/Si(1 0 0) wafers. The as-deposited oxide surfaces were found to be sufficiently smooth for direct wafer bonding for the Si control wafers but required a CMP step to reduce the RMS roughness below 1 nm for sSi wafers due to the fact that these wafers were already quite rough and this roughness was replicated upon HDP-CVD oxide deposition. The wafers with HDP-CVD oxides were bonded to thermally oxidized Si(0 0 1) handle wafers. The bonded pairs were annealed at 300 °C for 5 h and then at 500 °C for 2 h. The bonded interfaces were found to be almost free of voids (except sSi wafers which showed a few voids but these can be removed with more careful cleaning of the wafers prior to bonding) before and after the annealing up to 500 °C. Furthermore, the bonded wafers were found to be void- and bubble-free up to 800 °C for 1 h if an outgassing step was performed at 850 °C for 1 h prior to bonding. We conclude that the HDP-CVD oxide layers can be reliably utilized for the layer transfer of ultrathin sSi layers onto Si handle wafers for the fabrication of sSOI substrates.

Acknowledgements

The authors gratefully acknowledge the German Federal Ministry of Education and Research (BMBF) for financial support within the TeSiN project consortium (contract no. V03110). We are thankful to Mrs. S. Hopfe for the XTEM sample preparation and Dr. R. Scholz for the XTEM measurements. We are grateful to Dr. D. Webb, ATMI Inc., USA for providing high quality sSi/SiGe/Si substrates.

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