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Source engineering in short channel double gate vertical SiGe-MOSFETs

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Abstract

Transistor channel lengths are being continually scaled to smaller dimensions to improve the high-frequency performance and package density, which will lead to the introduction of sub-50 nm gate lengths in production in the near future. In this paper, the performance of a double gate (DG) vertical metal oxide semiconductor field effect transistor (MOSFET) using strained-SiGe as the channel has been analyzed using simulation. The advantages of the band gap engineering and the vertical structure are shown in terms of (a) independence of channel length, (b) independence of source-drain bias, (c) improved device characteristics (lower off-current), (d) reduction of short channel effects, and (e) suitability for low-power operation.

Keywords: SiGe; Heterojunction FET; Short channel effect; Double gate vertical MOSFET

1. Introduction

Over the last few decades, high packing density and enhanced performance of VLSI chips have been achieved through down scaling of the vertical metal oxide semiconductor field effect transistor (MOSFETs) successfully. Currently, sub-100 nm MOSFET devices are facing two fundamental limits: first one is technological in nature, lithographic resolution and doping confinement and the second one is related to the short channel effect (SCE) and drain-induced barrier lowering (DIBL). Although lithographic techniques such as electron beam lithography and X-ray lithography can be used in nm gate length regime, these processes are not economically viable.

Recently, the use of vertical transistors has gained a lot of interest as the channel length of the transistor is decided by epitaxial layer thickness and not by the photolithography [1]. De Meyer et al. [2] reported a novel device structure: the vertical advanced heterojunction MOSFET (VAHMOS). The main advantages of the vertical heterojunction transistors are, besides being easily fabricated with channel lengths below 100 nm, the device may have source/channel heterojunction to reduce the short channel effect and the drain-induced barrier lowering. For the p-MOSFETs, strained-SiGe source/Si channel was used. The purpose of using the heterojunction was to get a material-dependent barrier for the carriers in the off-state and thereby controlling the off-state current. This is one of the major advantages of the vertical advanced heterojunction MOSFETs. The suppressed SCE is related to the shape of the surface potential.

Bandgap engineering and, more specifically, the use of heterojunctions in the design of MOSFETs is still not fully explored. Use of double gate provides a two-fold improvement in drive current for same channel width of single gate MOSFET. Due to the fact that strained-SiGe

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has higher hole mobility, use of this material as channel further improves drive current. The higher strain in the source than the channel region provides a type-I band offset at the source/channel interface, which creates a "hard barrier" to the holes injecting from source to channel area and consequently can reduce the DIBL effect significantly. In this paper, we have studied the performance of SiGe-channel double gate vertical advanced heterojunction p-MOSFETs (DG-VAHMOS) using simulation.

2. Simulation

Several material parameters are essential for the device simulation, the most crucial of which are the band gap narrowing due to Ge fraction, electron affinity, and density of states, dielectric permittivity and the carrier mobility. Compressive strain in SiGe breaks the degeneracy between the heavy hole (HH) and light hole (LH) sub-bands at Γ-point and moves the split off (SO) sub-band further away in energy [3]. The HH sub-band moves up in energy than the LH sub-band as shown in Fig. 1a and become the preferential residence for the holes taking part in the current conduction. Based on the nonlocal empirical pseudopotential theory, Fischetti et al. [3] have shown that the reduction of both in-plane $\langle 1\,0\,0\rangle$ and out-of-plane $\langle 0\,0\,1\rangle$ heavy hole conductivity effective masses in compressively strained-SiGe will increase the hole mobility. In addition, the band splitting reduces the inter-valley hole scattering rate and consequently increases both the in-plane and out-of-plane hole mobilities. The higher in-plane hole mobility as well as the higher mobility normal to the growth plane (1 0 0) have also been predicted by Manku et al. [4] and they extracted the out-of-plane mobility enhancement factor as shown in Fig. 2.

In the simulation, the extracted in-plane and out-of-plane hole mobility enhancement in strained SiGe as a function of Ge mole fraction in the layer have been

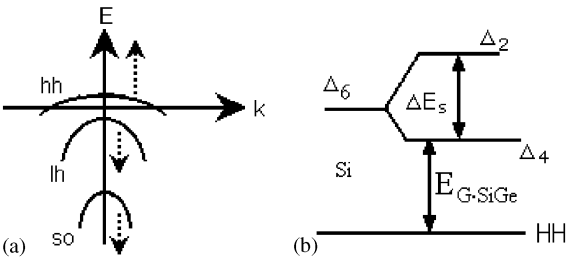

Fig. 1. (a) Valence band energy splitting in compressively strained SiGe and (b) indirect energy band gap of compressive strained SiGe layer.

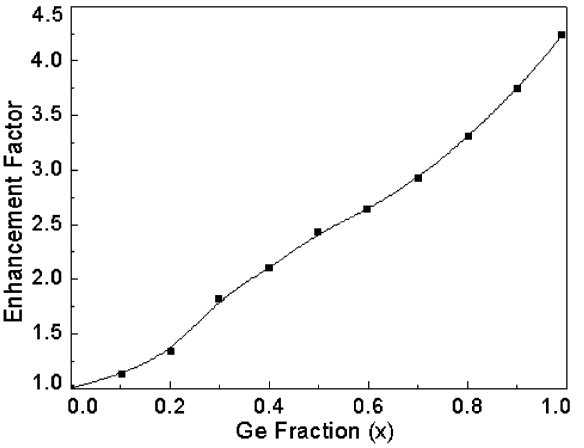

Fig. 2. The out-of-plane hole mobility enhancement factor.

modeled by the following empirical relations:

$$F_1 = (1 + 5.15x - 4.55x^2 + 1.45x^3), \tag{1}$$

$$F_2 = (1 + 2.93x - 0.78x^2 + 1.168x^3), \tag{2}$$

where x is the Ge mole fraction.

The enhancement factors essentially take into account the first-order effect of reduced carrier effective mass. The out-of-plane inversion layer hole mobility in compressively strained SiGe has been modeled by modifying the Lombardi mobility model [5] for Si as follows:

$$\frac{1}{\mu_{\mathrm{SiGe}}} = \frac{1}{\mu_{\mathrm{Si.CVT}} \times F_2} + \frac{1}{\mu_{\mathrm{alloy}}}, \tag{3}$$

where

$$\frac{1}{\mu_{\mathrm{Si.CVT}}} = \frac{1}{\mu_{\mathrm{ac}}} + \frac{1}{\mu_{\mathrm{b}}} + \frac{1}{\mu_{\mathrm{sr}}}, \tag{4}$$

where μ_{ac} is the carrier mobility limited by the scattering with the surface acoustics phonons, μ_{b} is the carrier mobility limited by the scattering with optical intervalley phonons, and μ_{sr} is the surface roughness scattering limited mobility.

The carrier mobility, μ_{alloy} has been approximated by Vogelsang et al. [6] as follows

$$\frac{1}{\mu_{\mathrm{alloy}}} = x(1-x)\ \exp(-7.86x)/124.1 \quad \text{for } x \Leftarrow 0.2 \tag{5}$$

and

$$\frac{1}{\mu_{\mathrm{alloy}}} = \exp(-2.68x)/2150 \quad \text{for } x > 0.2. \tag{6}$$

The mobility component, μ_{ac} in Eq. (4), which is the acoustic phonon scattering, is given by [5]

$$\mu_{\mathrm{ac}} = \left[\frac{BT}{E_\perp} + \frac{CN^\tau}{E_\perp^{1/3}}\right] T^{-1}, \tag{7}$$

where $E_\perp$ is the perpendicular electric field, N is the total doping concentration, T is the temperature.

The mobility component, μ_{sr} in Eq. (4), which is limited by the scattering, is given by [5]

$$\mu_{sr} = \frac{\delta}{E_\perp^2} \tag{8}$$

and the third mobility component, μ_b in Eq. (4), which is limited by the scattering with optical inter-valley phonons, from [5] is as follows

$$\mu_b = \mu_0 \exp(-P_c/N) + \frac{[\mu_{max}(T/300)^{-\gamma} - \mu_0]}{1 + (N/C_r)^\alpha} - \frac{\mu_1}{1 + (C_s/N)^\beta}. \tag{9}$$

The values for different parameters in Eqs. (7)–(9) can be obtained from [5].

For compressively strained SiGe (on Si), the in-plane four-fold (Δ_4) conduction bands (Δ_{100}) are lower in energy than the out-of-plane two-fold (Δ_2) conduction bands (Δ_{001}) [3]. The energy difference between the Δ_4 conduction band and HH valence band decides the indirect band gap [3] of compressively strained SiGe as shown in Fig. 1b. The reported data for band offset and band gap in Refs. [1,3] are used to construct the empirical expressions for indirect band gap and electron affinity for compressive strained $Si_{1-x}Ge_x$ as given below

$$E_G(Si_{1-x}Ge_x) = E_G(Si) - 0.74x \quad \text{for } x < 0.4, \tag{10}$$

where x is the Ge mole fraction.

The electron affinity of bulk-Si is equal to 4.17 eV. The change in the electron affinity has been modeled by using the conduction band offset (ΔE_c) created in strained layers and is given by

$$\chi(x) = \chi_{Si} + \Delta E_c. \tag{11}$$

For compressively strained $Si_{1-x}Ge_x$ the electron affinity can be analytically modeled as

$$\chi(Si_{1-x}Ge_x) = \chi(Si) + 0.196x - 0.396x^2 \quad \text{for } x < 0.6, \tag{12}$$

where x is the Ge mole fraction.

The schematic structure of the device used for simulation using Silvaco-ATLAS [7] is shown in Fig. 3. To reduce the DIBL, a type-I band offset between the $Si_{1-y}Ge_y$ (channel) and $Si_{1-x}Ge_x$ (source) ($x > y$) is used to create a "hard barrier" to the holes at source/channel interface. The source can be directly grown on Si or a graded-$Si_{1-z}Ge_z$ ($z < y$) can also be used as shown in Fig. 3. A gate oxide thickness of 5 nm and fixed oxide charges at Si/SiO_2 and Si/SiGe interfaces were taken to be 5×10^{10} cm^{-2} in simulation. Associated other parameters used in device simulation are given in Table 1.

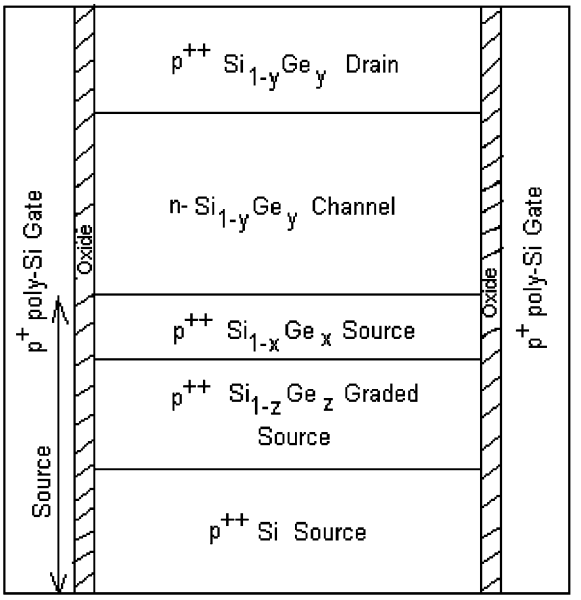

Fig. 3. Schematic diagram of the DG-VAHMOS.

Table 1
Device parameters used in simulation

Layer	Doping (cm^{-3})	Thickness (nm)	Ge %
Drain	1×10^{20}	200	10
Channel	1×10^{18}	100	10
SiGe-source	1×10^{20}	30	30
SiGe graded source	1×10^{20}	15	0 to 30 upwards
Si source	1×10^{20}		

3. Results and discussion

The decrease in potential barrier due to a change in the drain potential from −1.5 to −5.0 V in homojunction ($x = y$) MOSFET is schematically shown in Fig. 4. Due to this reason, the magnitude of the threshold voltage of the transistor reduces as the magnitude of the drain potential increases, which results in higher sub-threshold leakage power dissipation. In DG-VAHMOS, a "hard barrier", as shown in Fig. 5, to the holes is created at the source–channel interface by utilizing the type-I band offset in $Si_{1-x}Ge_x/Si_{1-y}Ge_y$ system. The simulated surface potential profile from source to drain (not shown) shows a significant reduction in the DIBL. The simulated drain characteristics of a 100 nm channel SiGe DG-VAHMOS and its homojunction counterpart are shown in Fig. 6a. Current does not saturate in the homojunction transistors, as the threshold voltage

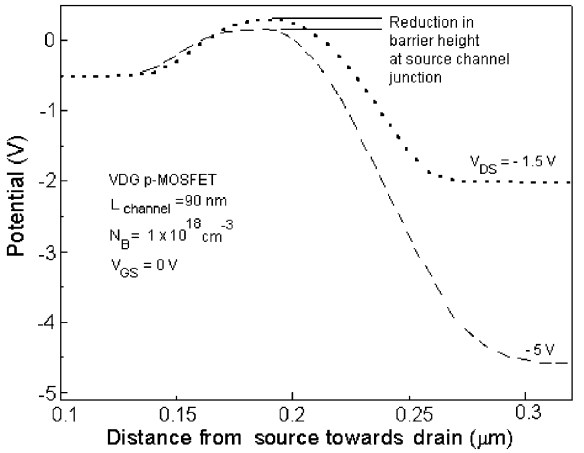

Fig. 4. Simulated potential profile from source towards drain inside a 90 nm homojunction ($x = y = 0$) double gate vertical MOSFET with different drain bias.

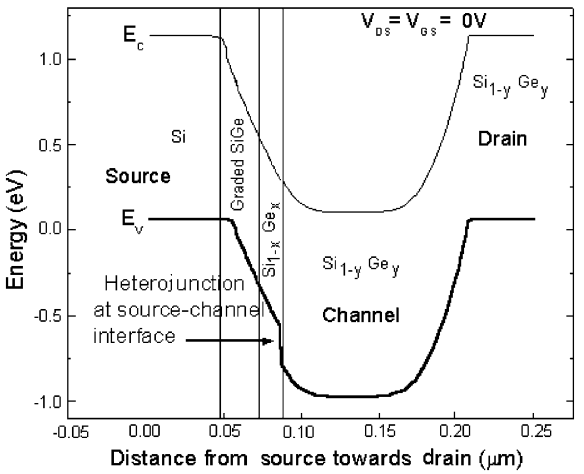

Fig. 5. Simulated band diagram inside the 90 nm SiGe channel DG-VAHMOS.

decreases with the drain bias. In the case of heterojunction, due to an extra barrier at the source/channel interface, excellent saturation in the drain characteristics is observed. Sub-threshold slope in the homojunction case is found to be 92 mV/decade and it decreases in case of heterojunction as expected to 90 mV/decade.

To benchmark the SiGe material model parameters used in simulation, we show in Fig. 6b, a comparison of the simulation results with the reported experimental device data from Ref. [8] for a strained SiGe channel vertical MOSFET. A good fit between the simulated and experimental drain currents shows the soundness of the modeling approach used.

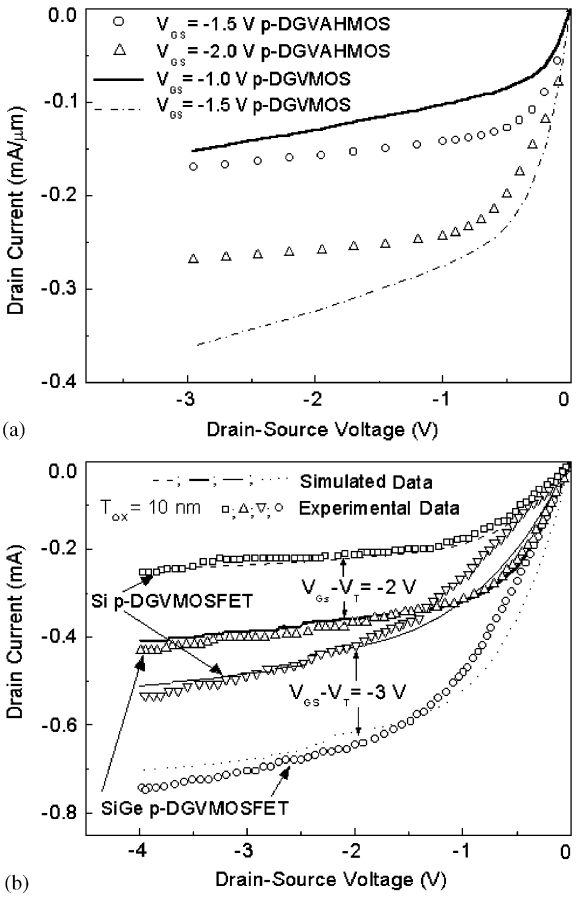

Fig. 6. (a) Output characteristics of a DG-VAHMOS with 10% Ge in the channel and its homojunction counterpart for a channel doping of $10^{18}\,cm^{-3}$ and (b) simulated and experimental [8] output characteristics of Si and graded SiGe p-MOSFETs.

4. Conclusion

In summary, we have shown using simulation that vertical DG-VAHMOS transistors with a compressively strained SiGe channel and ultra-short length of 90 nm may be realized and significant performance enhancements can be achieved in terms of higher saturation drain current, lower short channel effect, and lower drain-induced barrier lowering. The transistors show fairly good device characteristics when the surface potential profile between the source and drain is optimized. Due to the small device dimensions and negligible short-channel effects as apparent in the output characteristics, these devices may find applications in future generation CMOS using vertical structures in SiGe hetero-FET technology.

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