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Characterization of reactions at titanium/nickel silicide interface using X-ray photoelectron spectroscopy and transmission electron microscopy

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Abstract

TiN/Ti/NiSi/Si multilayer system is of great technological importance for complementary metal-oxide-semiconductor (CMOS) device fabrication. Interfacial reactions in this multilayer system play a critical role in determining the contact resistance and affect silicon consumption, a key issue in shallow junction structures. In this report, interfacial reactions in TiN/Ti/NiSi/Si multilayer systems, with a focus on Ti/NiSi interface, were characterized using X-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM) and four-point probe measurements. Impact of thermal treatment temperatures was investigated.

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1. Introduction

As complementary metal-oxide-semiconductor (CMOS) devices scale to sub-0.1 μm regime, the self-aligned silicide (SALICIDE) contact technology increasingly becomes an integral part of ultra-shallow junctions [1,2]. $TiSi_2$, $CoSi_2$ and NiSi are the three most important silicide systems for CMOS fabrication. Although $TiSi_2$ is widely used in $\geq$0.25 μm technology nodes, the line width dependence of C49 to C54 phase transition of $TiSi_2$ limits its application for CMOS devices of smaller sizes. $CoSi_2$ formation is less dependent on the poly-silicon gate line width and is stable for the thermal budget used in most CMOS devices. $CoSi_2$ is currently the dominant silicide used in SALICIDE applications. The main disadvantage of $CoSi_2$ is that, among the three common silicides, it consumes the most Si during silicide formation. The excess Si consumption is a problem for ultra-shallow junctions. NiSi formation is also less dependent on poly-silicon gate line width. In addition, NiSi consumes the least amount of Si during silicide formation. NiSi can be formed at relatively low temperature (400–550 °C), while $TiSi_2$ and $CoSi_2$ both

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require a formation temperature higher than 700 °C. The lower process temperature reduces dopant depletion of the underneath junctions, which is another major advantage of NiSi. However, NiSi is also the least stable silicide. Thermal budget after NiSi formation needs to be kept below 600 °C to prevent NiSi silicide from agglomeration and transformation into the high resistivity and thermodynamically stable phase of $NiSi_2$. Nevertheless, as source/drain junctions are getting shallower, NiSi becomes the most attractive candidate for the next generation SALICIDE application due to its low Si consumption, despite its instability at high process temperatures (≥600 °C).

NiSi is normally covered with a native oxide layer upon exposure to air. In a typical CMOS device process flow, a Ti layer is deposited as a liner in contact with NiSi to reduce the surface oxide. Contacts between transistors and the first layer metallization lines are made by chemical vapor deposited (CVD) W, which uses WF_6 as a precursor. In order to prevent adverse chemical reactions between Ti and WF_6, a TiN diffusion barrier is deposited after Ti and before CVD W. Therefore, TiN/Ti/NiSi/Si is a real multilayer system of great technological importance for CMOS device fabrication. In this report, interfacial reactions from TiN/Ti/NiSi/Si multilayer systems, with a focus on Ti/NiSi interface, as a function of different rapid thermal annealing (RTA) temperatures are characterized by X-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM) and sheet resistance measurement.

2. Experimental

Blanket NiSi (17 nm) films on Si(1 0 0) were used as substrate for this study. A Ti film of 16 nm was deposited by ionized sputtering, followed by a TiN film of 9 nm using a chemical vapor deposition process. Both Ti and TiN depositions were performed in a commercial deposition cluster tool (Applied Materials, Endura 5500) with a background pressure of 1×10^{-9} Torr. The wafers were then processed through rapid thermal annealing at different temperatures (580, 550, 500, and 450 °C) for 30 s. The processed wafers were then characterized by X-ray photoelectron spectroscopy and transmission electron microscope. XPS has the advantage in quantifying relative atomic concentrations, which is complemented by structural information obtained from TEM. XPS analysis was carried out in a Physical Electronic/5700 system using monochromated Al Kα radiation. For TEM analysis, a FEI CM200 system was used. Sheet resistance was measured by four-point probe.

3. Results and discussion

3.1. XPS depth profiling

Fig. 1(a) shows the XPS depth profile from the as-deposited wafer with 9 nm TiN/16 nm Ti on NiSi. The NiSi layer is present between the Si substrate and Ti layer. Ni and Si distributions are relatively the same as those of the as-received NiSi wafer. This indicates that the TiN/Ti deposition does not affect the stoichiometry of NiSi layer. Oxygen distribution is evenly distributed within the Ti layer, instead of pile-up at the Ti/NiSi interface. This is probably due to the relatively high temperature (>400 °C) used in CVD TiN deposition process. The oxygen originates from the surface oxide on top of the as-received NiSi. Fig. 1(b) is the XPS depth profile from the as-deposited wafer after RTA at 580 °C for 30 s. It is clear that Ti reacts with underlying NiSi to form $TiSi_x$, in which NiSi is broken and becomes Si-poor. The Si-poor Ni atoms react with more Si from the junctions and result in a Si-rich silicide, $NiSi_{1+x}$ (Ni:Si ~ 2:3). Note, excess Si from source/drain junctions is consumed during the above RTA process, in addition to that consumed during the original NiSi formation process. Oxygen piles up at the $Ti/TiSi_x$ interface after the 580 °C RTA process. This suggests that Ti diffuses quickly to react with Si, in which oxygen is left to pile-up. It is also noticed that N signal extends further into the Ti layer. This is probably due to N_2 diffusing through CVD TiN and reacting with the under layer Ti in the RTA N_2 ambient. Fig. 1(c) shows the XPS depth profile of the as-deposited wafer after RTA at 500 °C for 30 s. The XPS depth profiles of the as-deposited wafer after RTA at 550 °C for 30 s (not included here) exhibit distributions in-between Fig. 1(b) and (c). In Fig. 1(c), it is seen that the thickness of the interlayer consisting of Ti and Si is significantly narrowed, with oxygen

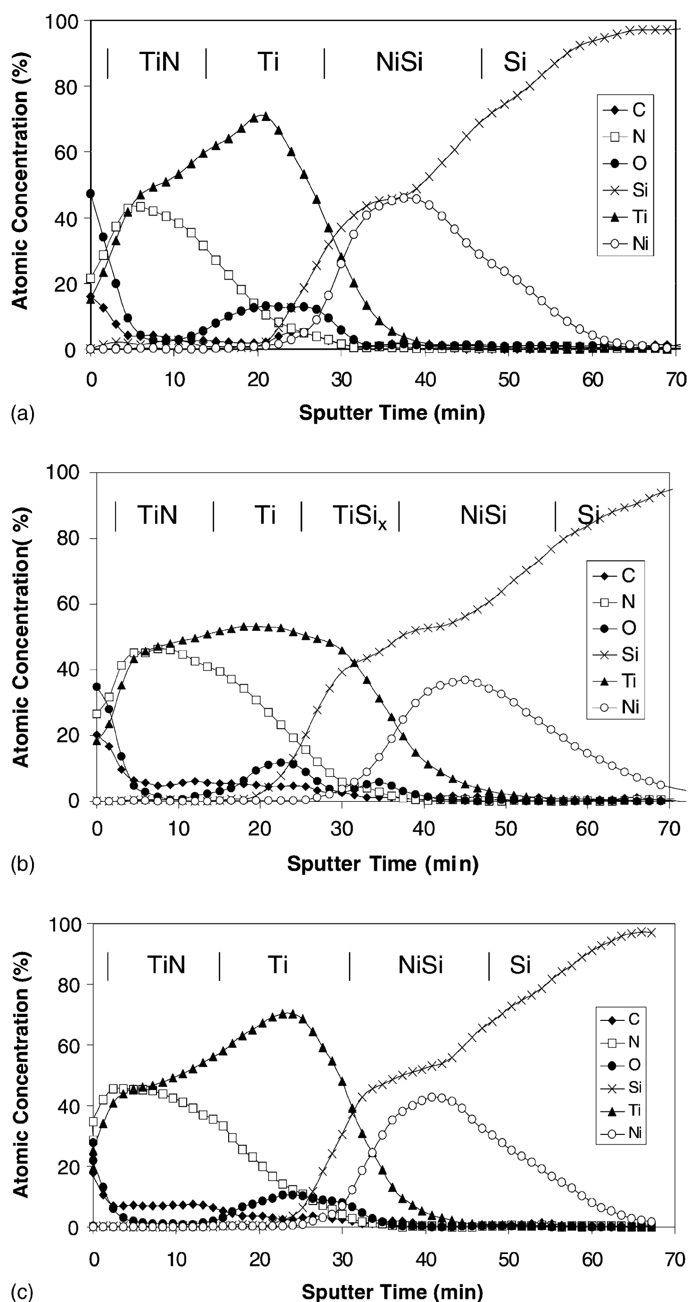

Fig. 1. XPS depth profiles: (a) as-deposited 9 nm CVD TiN/16 nm IMP Ti/NiSi wafer; (b) as-deposited wafer after RTA at 580 °C; (c) as-deposited wafer after RTA at 500 °C.

being distributed evenly through the Ti layer. The nickel silicide region is still Si-rich. The XPS depth profile of the as-deposited wafer after RTA at 450 °C for 30 s shows similar profiles to that of Fig. 1(a). In summary, with RTA temperature ≥550 °C, $TiSi_x$ interlayer is formed between Ti and NiSi layers. In addition, NiSi is transformed to Si-rich silicide, $NiSi_{1+x}$. With RTA temperature of 500 °C, no significant

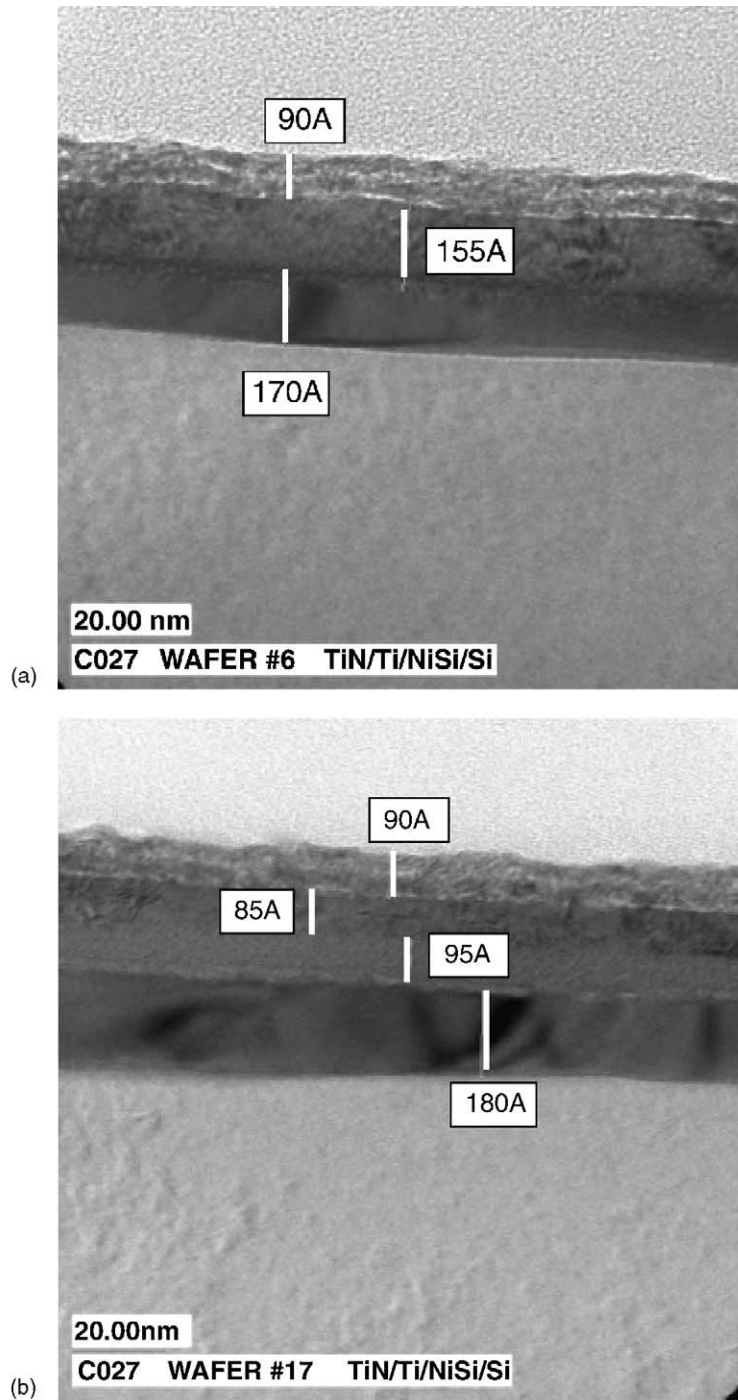

Fig. 2. TEM cross-section images: (a) as-deposited 9 nm CVD TiN/16 nm IMP Ti/NiSi wafer; (b) as-deposited wafer after RTA at 580 °C; (c) as-deposited wafer after RTA at 550 °C.

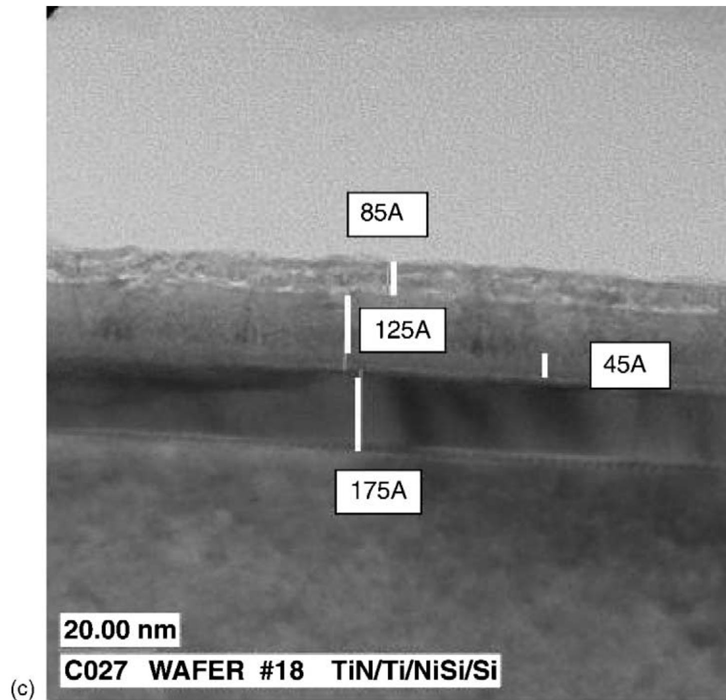

Fig. 2. (*Continued*).

amount of $TiSi_x$ interlayer is formed, however, NiSi is still transformed to Si-rich silicide. At RTA temperature of 450 °C, the formation of $TiSi_x$ and $NiSi_{1+x}$ is prevented, therefore, the integrity of NiSi is preserved.

3.2. TEM cross-section images and sheet resistance measurement

Fig. 2(a)–(c) shows the TEM cross-section images of the as-deposited TiN/Ti/NiSi wafer and the wafers after RTA at 580, 550 °C, respectively. After TiN/Ti deposition, three separate layers of TiN, Ti and NiSi are shown in Fig. 2(a), with the Ti layer measured 15.5 nm and the NiSi layer measured 17 nm. Fig. 2(b) shows the TEM cross-section image of the wafer after RTA at 580 °C, where four layers are clearly present. Under the top TiN layer, the Ti layer thickness is reduced to 8.5 nm and the $TiSi_x$ interlayer is measured 9.5 nm. The NiSi layer thickness slightly increases to 18 nm possibly due to the added Si. Fig. 2(c) shows the TEM cross-section image of the as-deposited wafer after RTA at 550 °C, where again four layers are present with a much thinner $TiSi_x$ interlayer than that in Fig. 2(b). The thickness of the Ti layer, the $TiSi_x$ interlayer and the NiSi layer in Fig. 2(c) are measured 12.5, 4.5 and 17.5 nm, respectively. TEM cross-section images of the wafers after RTA at 500 and 450 °C are similar to Fig. 2(a). This result supports the XPS depth profiling analyses, indicating that, interface reaction occurs between Ti and NiSi to form $TiSi_x$ at RTA temperature $\geq$550 °C.

Fig. 3 shows the sheet resistance variations of the TiN/Ti/NiSi wafers as a function of RTA temperature. As seen in the figure, with RTA temperatures $\geq$550 °C, sheet resistance of the TiN/Ti/NiSi multilayer structure increases dramatically. This increase in resistance further supports the above XPS depth profiling and TEM cross-section analyses. With RTA temperatures $\geq$550 °C, high resistance $TiSi_x$ is formed, which is not the low resistance and stoichiometric $TiSi_2$. With RTA temperature increasing from 550 to 580 °C, the thickness of the $TiSi_x$ interlayer increases. This increases the sheet resistance significantly. The slight increase of sheet resistance after RTA at 500 °C is probably due to the enrichment of Si that forms $NiSi_{1+x}$.

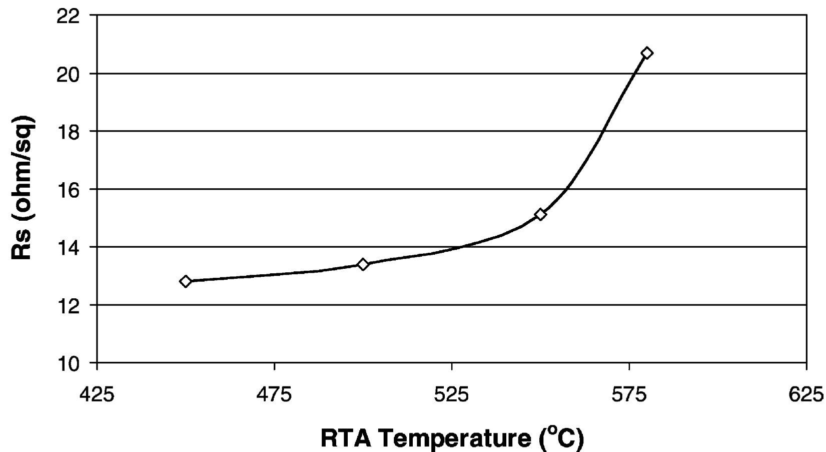

Fig. 3. Sheet resistance variations of the 9 nm CVD TiN/16 nm IMP Ti/NiSi wafers as a function of RTA temperature.

4. Conclusions

The impacts of TiN/Ti deposition and subsequent thermal treatments on NiSi have been investigated using XPS, TEM and sheet resistance measurement. NiSi surface is covered with a native oxide layer upon exposure to air. This oxide layer can be reduced by depositing TiN/Ti layer, followed by RTA. However, if the RTA temperature is high ($\geq$550 °C), Ti atoms can destroy the integrity of NiSi by taking Si from Ni to form $TiSi_x$. This $TiSi_x$ film is not the stoichiometric $TiSi_2$ phase and has high resistivity, which results in high contact resistance. In addition, the Si-poor Ni atoms then diffuse to the junctions and react with more Si to form nickel silicide. In this process, more Si is consumed in addition to that consumed in the original NiSi formation process. When the Ti/NiSi interfacial system is processed in an optimal RTA temperature window, the interfacial oxide is reduced to form low resistance contacts, while the RTA temperature is low enough to preserve the integrity of NiSi and to prevent high resistivity $TiSi_x$ from formation.

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