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# Device-quality GaN–dielectric interfaces by 300 °C remote plasma processing

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**Abstract**

In previous studies, device-quality Si–$SiO_2$ interfaces and dielectric bulk films ($SiO_2$) were prepared using a two-step process; (i) remote plasma-assisted oxidation (RPAO) to form a superficially interfacial oxide (~0.6 nm) and (ii) remote plasma enhanced chemical vapor deposition (RPECVD) to deposit the oxide film. The same approach has been applied to GaN–$SiO_2$ system. Low-temperature (300 °C) remote $N_2$/He plasma cleaning of the GaN surface, and the kinetics of GaN oxidation using RPAO process and subcutaneous oxidation during the $SiO_2$ deposition using an RPECVD process have been investigated from analysis of on-line Auger electron spectroscopy (AES) features associated N and O. Compared to single-step $SiO_2$ deposition, significantly reduced defect state densities are obtained at the GaN–dielectric interfaces by independent control of GaN–$GaO_x$ ($x \sim 1.5$) interface formation by RPAO, and $SiO_2$ deposition by RPECVD.
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*Keywords:* GaN–dielectric interfaces; Surface leaning; Subcutaneous oxidation; $Ga_2O_3$; $SiO_2$; MOSd devices

## 1. Introduction

GaN has emerged as important material for optoelectronic and high-temperature/high power/high frequency device applications. As such, GaN–dielectric insulators for gate dielectrics [1] and surface passivation layers [2], as well as surface cleaning [3,4] have become important issues in device processing. When dielectric layers are formed on a GaN surface by deposition rather than oxidation, the pre-deposition cleaning of the GaN surface is a critical requirement because the initially prepared surface forms the buried device interface. The in situ deposition of the epitaxially grown films, including lattice-matched heterojunctions with other group III-nitride materials, have identified the potential importance for GaN-based metal–insulator–semiconductor (MIS) technology. Deposited amorphous $SiO_2$ and $Al_2O_3$ have been the two most promising insulators for III–V semiconductor, mainly because of their wide band gaps. $Si_3N_4$ is another choice when substrate oxidation during dielectric deposition must be avoided.

When $SiO_2$ thin films are deposited directly onto Si, Ge, GaAs and CdTe using remote plasma enhanced chemical vapor deposition (RPECVD), these substrates were oxidized superficially by plasma-activated species during the initial stages of film deposition [5]. These parasitic reactions, or *subcutaneous oxidation processes*, during thin film deposition degrade the electrical characteristics of the interfaces. To prevent subcutaneous oxidation of GaAs and Ge, a thin sacrificial Si layer was deposited before the deposition of $SiO_2$ thin film [5]. Improved surface passivation of GaAs was

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obtained by removal of $As_2O_3$ and subsequent formation of a $Ga_2O_3$ film [6]. To prepare a device-quality Si–$SiO_2$ interface and dielectric bulk film ($SiO_2$), a superficially thin Si oxide layer (~0.6 nm) was formed on silicon substrate by a remote plasma-assisted oxidation (RPAO) process, and the remainder of the oxide layer is deposited by the RPECVD process [7,8]. The same RPAO–RPECVD process has been applied to SiC–$SiO_2$ [9] and GaN–$SiO_2$ [10], respectively.

In this work, a low-temperature plasma-assisted N ion cleaning process, the kinetics of GaN oxidation and occurrence of subcutaneous oxidation of GaN during plasma enhanced deposition of $SiO_2$ films have been studied using Auger electron spectroscopy (AES) measurements. Additionally, we report on the effect of subcutaneous oxidation the on degradation of electrical characteristics of GaN metal-oxide–semiconductor (MOS) capacitors.

## 2. Experimental

An epitaxial GaN(0 0 0 1) layer was directly grown on the *c*-plane of sapphire by hydride vapor phase epitaxy (HVPE) using commercial TDI wafers. Silicon was used as n-type dopant, and the thickness of the GaN epitaxial layer was 5 μm. These GaN layers had a electron concentrations of $(5-10) \times 10^{17}$ $cm^{-3}$. The 2 in. GaN/sapphire wafers were degreased in acetone, and then methanol, each for 20 min. A standard RCA clean was followed by etching in 1:5 $NH_4OH$:$H_2O$ solutions at 60–80 °C (or in HCl-based solutions). Following this, GaN samples were loaded into a multi-chamber system [7–10], which provided chambers for remote plasma-assisted processing and on-line AES measurements. The GaN sample was first exposed to reactive species from a remote $N_2$/He discharge at 0.02–0.3 Torr. The in situ cleaned GaN surface was then oxidized by an RPAO process using a He/$O_2$ source gas mixture [11]. For the $SiO_2$ deposition, the flow rates for plasma excited $O_2$ and He, and down-stream injected 2%-$SiH_4$ in He were, respectively 60, 200 and 10 sccm. The process pressure, substrate temperature and plasma power for both the oxidation and $SiO_2$ deposition were 0.3 Torr, 300 °C and 30 W at 13.56 MHz, respectively. The experimental procedure was to alternate AES measurements using a 3 keV electron beam with the $SiO_2$ depositions of 20 s. Post-oxide deposition annealing (POA) was carried out at 900 °C for 30 min in an $N_2$ atmosphere. For the fabrication of GaN MOS capacitors, a 300 nm Al layer was evaporated after the formation of the gate dielectric. After an electrode area was defined by a conventional lithography process, post-metallization annealing (PMA) was performed at 400 °C for 30 min in forming gas ($N_2$/$H_2$).

## 3. Results and discussion

Fig. 1 shows differential AES spectra of (i) as-loaded GaN surface (after etching in 1:5 $NH_4OH$:$H_2O$ solutions), and $N_2$/He plasma treated GaN surface at 300 °C for 15 min at (ii) 0.02, (iii) 0.1 and (iv) 0.3 Torr, respectively. The $N_2$/He plasma treatment in the pressure range from 0.02 to 0.3 Torr reduced residual C below AES detection. Reducing the process pressure of $N_2$/He plasma from 0.3 to 0.02 Torr, the

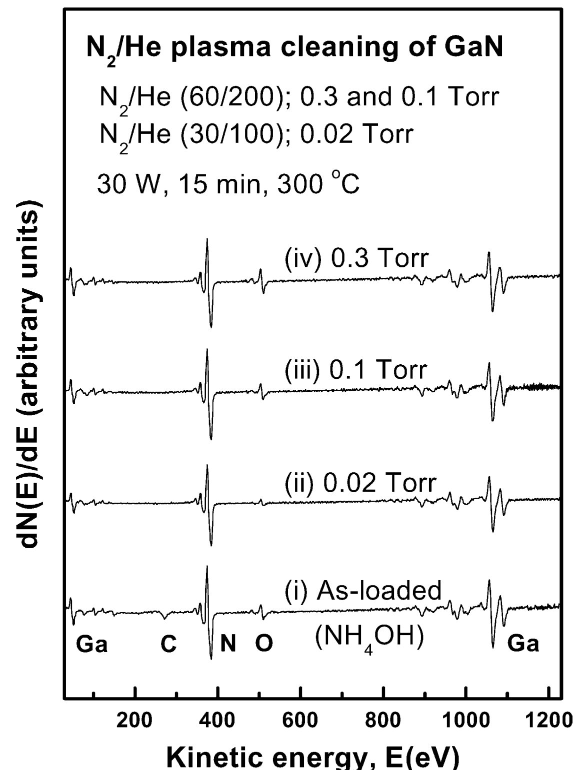
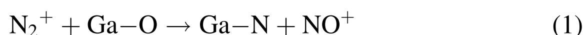



Fig. 1. Differential AES spectra of (i) as-loaded (after etching in 1:5 $NH_4OH$:$H_2O$), and $N_2$/He plasma treated GaN surface at 300 °C for 15 min at (ii) 0.02, (iii) 0.1 and (iv) 0.3 Torr, respectively.

AES peak ratio of O KLL and N KLL (O/N) was reduced to a limiting value of ~0.06, which is approximately the same as that of a GaN surface obtained by annealing in $NH_3$ at 860 °C [4]. By reducing the process pressure from 0.3 to 0.02 Torr during the $N_2$/He clean, the O coverage on GaN surface ($t_{ox}$) obtained using integrated Auger intensity area ratio of each element [3], decreased from ~0.5 to ~0.1 monolayer (ML). Wet chemical treatment using 1:1 HCl:$H_2O$ and 3:1 HCl:$HNO_3$ solutions were also used before $N_2$/He plasma treatment. As shown in Fig. 2, each wet chemical treatment showed differences in the amounts of residual impurities, but the in situ $N_2$/He plasma treatment at 0.02 Torr reduced C and Cl below AES detection as well as the AES O/N ratio to ~0.06. Decreasing the pressure of remote $N_2$/He plasma process from 0.3 to 0.1 Torr, the active nitrogen species change from neutral N atoms to $N_2^+$ ions [8,12]. The enhanced O dissociation of GaN surface at 0.02 Torr can be attributed to the increase of charged particles such as the $N_2^+$ ion. It is proposed here that the $N_2^+$ ion reacts with O bonded to Ga atoms on the GaN surface in the following atom exchange reaction, which is favored by the increased bond energy of $NO^+$ with respect to $N_2^+$,



$$N_2^+ + \text{Ga}{-}\text{O} \rightarrow \text{Ga}{-}\text{N} + NO^+ \quad (1)$$

Following the low-temperature $N_2$/He plasma-assisted cleaning at 0.02 Torr, the interface and dielectric layer are formed by a two-step process, or RPAO–RPECVD process. The first step is plasma-assisted oxidation process using He/$O_2$ source gas mixture that forms an ultra-thin $Ga_2O_3$ layer on the GaN surface. The kinetics of GaN oxidation were determined from analysis of on-line AES features associated with N and O [8,11]. Fig. 3 shows log–log plots of the oxide

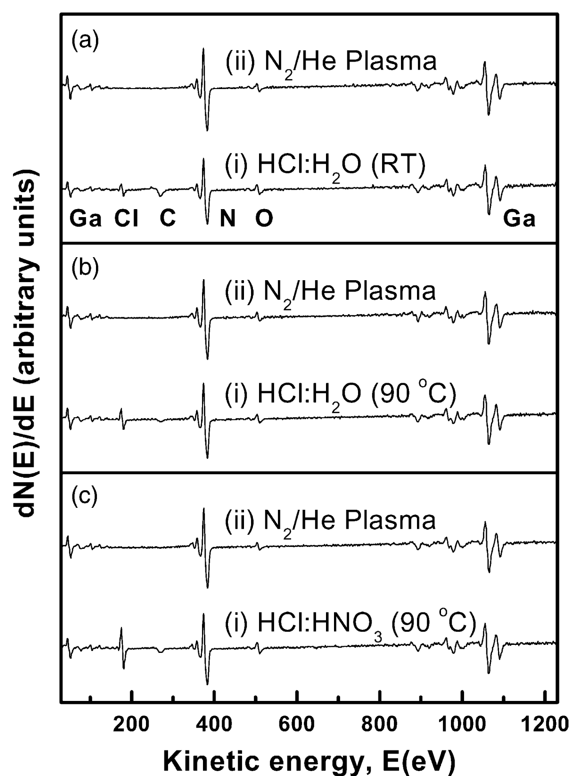



Fig. 2. Differential AES spectra of GaN surface after etching in (a) 1:1 HCl:$H_2O$ (RT), (b) 1:1 HCl:$H_2O$ (90 °C) and (c) 3:1 HCl:$HNO_3$ (90 °C). After in situ $N_2$/He plasma treatment at 0.02 Torr, C and Cl were reduced below AES measurement limit and O KLL/N KLL reduce to ~0.06 regardless of varied wet chemical treatments.

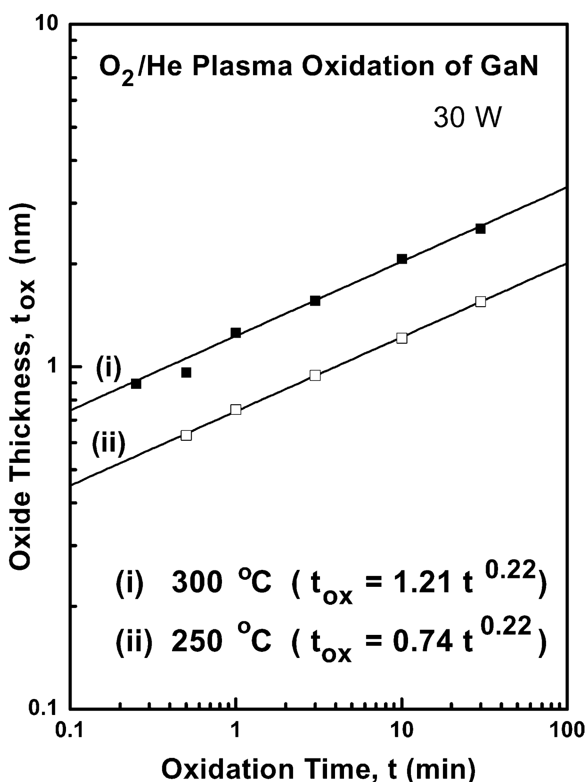



Fig. 3. Log–log plots of the oxide thickness ($t_{ox}$) as a function of oxidation time ($t$) for the RPAO process using $O_2$ source gas at 250 and 300 °C, respectively. The straight lines connecting the data points represent a power-law dependence, i.e. $t_{ox} = \tau_o t^{\beta}$, where $\tau_o$ and $\beta$ are fitting parameters.

thickness ($t_{ox}$) versus oxidation time ($t$) for the RPAO process at 250 and 300 °C, respectively. This process is self-limiting with lower-law kinetics similar to those for the plasma-assisted oxidation of Si and SiC [8,9]. The oxide thickness versus oxidation time relation is fitted by a lower-law function of the form, $t_{ox} = \tau_o t^{\beta}$, where $\tau_o$ and $\beta$ are fitting parameters; $t_{ox} = 1.21t^{0.22}$ (300 °C) and $t_{ox} = 0.74t^{0.22}$ (250 °C), respectively. The exponential constant, 'β' of the GaN oxidation at 250–300 °C (~0.22) is smaller than the corresponding exponential constants for Si (~0.28) [8] and SiC (~0.40) [9].

To demonstrate the occurrence of subcutaneous oxidation of GaN during deposition of $SiO_2$ using the RPECVD process, two different process sequences, shown in Fig. 4, were compared: (i) a direct deposition of $SiO_2$ on GaN using RPECVD and (ii) two-step process, i.e. RPAO process to form a superficially thin oxide layer (~1.0 nm) and deposition of $SiO_2$ on GaN using RPECVD process. Fig. 5 shows a comparison of oxide thickness as a function of $SiO_2$ deposition time. The oxide thickness of GaN samples was also obtained from analysis of on-line AES features associated with N and O [8,11]. Increasing the $SiO_2$ deposition time, the difference of oxide thickness between two samples was gradually reduced from the initial value of ~1 nm to ~0.3 nm.

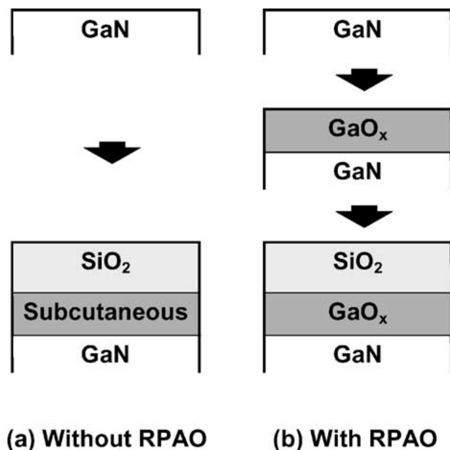



Fig. 4. Two different process sequences were used to demonstrate the presence of subcutaneous oxidation of GaN during deposition of $SiO_2$. (a) A direct deposition of $SiO_2$ on GaN using RPECVD process and (b) two-step process, i.e. RPAO process to form a superficially thin oxide layer (~1.0 nm) and deposition of $SiO_2$ on GaN using RPECVD process.

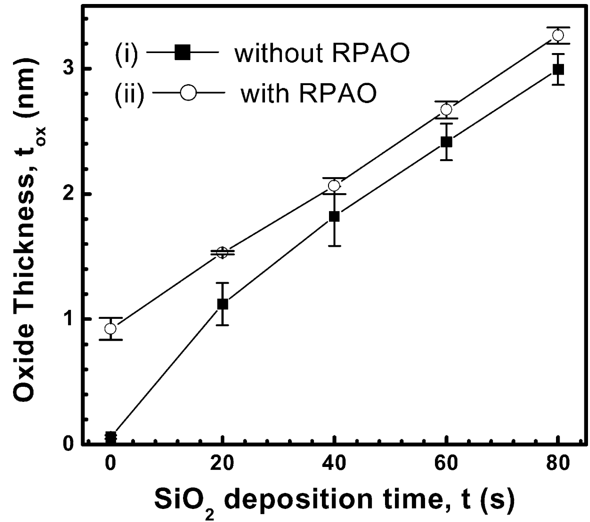



Fig. 5. Comparison of determined oxide thickness of GaN sample (i) without RPAO and (ii) with RPAO as a function of $SiO_2$ deposition time.

This reduction indicates that ~0.7 nm of $GaO_x$ was formed during the direct $SiO_2$ deposition on GaN sample without RPAO due to the subcutaneous oxidation process. The GaN samples with RPAO showed nearly linear $SiO_2$ deposition rate. This means that negligible subcutaneous oxidation occurred, and

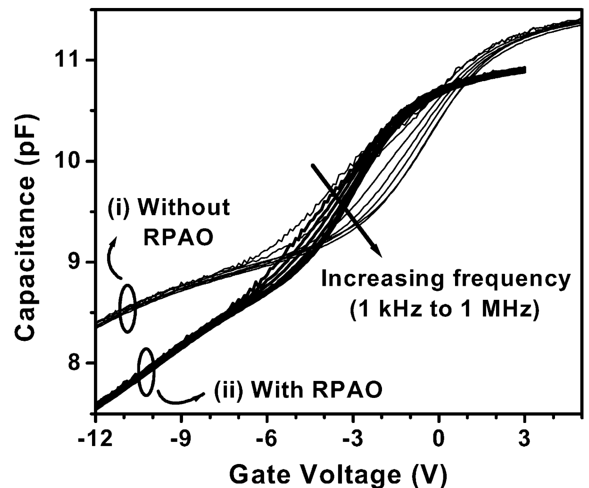



Fig. 6. The frequency dependence (from 1 kHz to 1 MHz) of the $C$–$V$ characteristics of GaN MOS capacitors (i) without RPAO and (ii) with RPAO.

Table 1
The characteristics of GaN MOS capacitors (i) without RPAO and (ii) with RPAO

| | $t_{ox}$ (nm) | $\Delta V_{FB}$ (V) | $N_f$ (cm$^{-2}$) | $D_{it}$ (cm$^{-2}$ eV$^{-1}$) |
|---|---|---|---|---|
| (i) Without RPAO | 31.2 | 2.0 | (−) $1.4 \times 10^{12}$ | $2 \times 10^{12}$ |
| (ii) With RPAO | 29.9 | −0.5 | (+) $3.5 \times 10^{11}$ | $3 \times 10^{11}$ |

$N_f$ is the oxide fixed charge obtained from the flat band voltage shift ($\Delta V_{FB}$), and $D_{it}$ is the density of interface state densities obtained from the Terman's method.

~1.0 nm of $GaO_x$ using RPAO process can inhibit the subcutaneous oxidation of GaN during the $SiO_2$ deposition by RPECVD.

Fig. 6 shows the frequency dependence ( from 1 kHz to 1 MHz) of the capacitance–voltage ($C$–$V$) characteristics of GaN MOS capacitors using $SiO_2$ thin films (~30 nm) (i) without RPAO and (ii) with RPAO (or ~1 nm $GaO_x$), respectively. The gate voltage was swept from accumulation (positive voltage) to depletion (negative voltage) at room temperature in the dark. Compared to the MOS sample without RPAO, the sample with RPAO showed small flat band voltage shift ($\Delta V_{FB}$) at 1 MHz and weak frequency dependence of the capacitance. The characteristics of GaN MOS capacitors (i) without RPAO and (ii) with RPAO were compared as listed in Table 1. In the evaluation of expressions for theoretical $C$–$V$ curves [13], the same fundamental constants in previous report [14] were used. The interface state densities ($D_{it}$) of both samples were calculated from Terman's method [13].

The minimum values of $D_{it}$ were $3 \times 10^{11}$ cm$^{-2}$ eV$^{-1}$ for with RPAO samples and $2 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$ for without RPAO samples, respectively. These $C$–$V$ characteristics indicate that fixed oxide charge and the density of interface trappings states can be reduced by the two-step remote plasma-assisted oxidation–deposition process.

## 4. Summary

An $N_2$/He plasma treatment at low-temperature (300 °C) removes residual C and Cl on GaN surface below AES detection, and reduces the AES peak ratio of O KLL and N KLL (O/N) to ~0.06 (or ~0.1 monolayer of oxygen coverage of GaN surface). The kinetics of GaN oxidation were determined from analysis of on-line AES features associated with Ga, N and O, and can be fit by an empirical power-law function. An on-line AES study indicates that ~0.7 nm of $GaO_x$ was formed during the direct $SiO_2$ deposition on GaN sample due to a subcutaneous oxidation process. Using a two-step process that provides separate and independent control of the interface, an ultra-thin $Ga_2O_3$ interfacial oxide, and the $SiO_2$ dielectric, a low interface state density of GaN MOS system was achieved.

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