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Advanced etching of silicon based on deep reactive ion etching for silicon high aspect ratio microstructures and three-dimensional micro- and nanostructures

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Abstract

Different processes involving an inductively coupled plasma reactor are presented either for deep reactive ion etching or for isotropic etching of silicon. On one hand, high aspect ratio microstructures with aspect ratio up to 107 were obtained on sub-micron trenches. Application to photonic MEMS is presented. Isotropic etching is also used either alone or in combination with anisotropic etching to realize various 3D shapes.
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1. Introduction

Less than 10 years ago, inductively coupled plasma (ICP) reactors have been introduced for silicon reactive ion etching (RIE) process leading to the deep reactive ion etching (DRIE) technique. The main novelties on these rather new ICP-RIE systems are the following:

- Separation of the main plasma from the wafer
- A higher plasma density
- Improved Radio Frequency RF-power supply
- Improved performance for pumping and mass-flow systems
- Pulsed Low Frequency LF substrate biasing
- New chemistry and new process (Bosch and cryogenic)

These hardware and process novelties led to improved performances, for instance:

- Higher selectivity for deep etching (DRIE)
- Higher aspect ratio (AR)
- Higher etching rate, either for anisotropic or isotropic etching
- Reduction of parasitic effects: notching, aspect ratio dependent Etching (ARDE), etc

The microfabrication of high aspect ratio microstructures (HARMS) is the main benefit of these technologies with numerous applications in the field of MEMS. There are two main ways of achieving HARMS by DRIE. The most popular way is the 'Bosch process', a patented process developed by Robert Bosch GmbH [1], which is based on alternating multiple steps of etching and sidewall passivation. The main alternative is the 'cryogenic process', relying on cooling the stage and silicon to cryogenic temperatures using liquid nitrogen [2,3]. In this work, both processes are studied, sometimes in isotropic conditions, in order to obtain unusual shapes or unusual feature sizes.

2. Sub-micron HARMS

2.1. Ultra-high aspect-ratio (AR) on sub-micron-wide trenches

Motivated by the need of fabricating silicon HARMS for nanophotonic applications [4,6], we developed a technological process for manufacturing deep trenches

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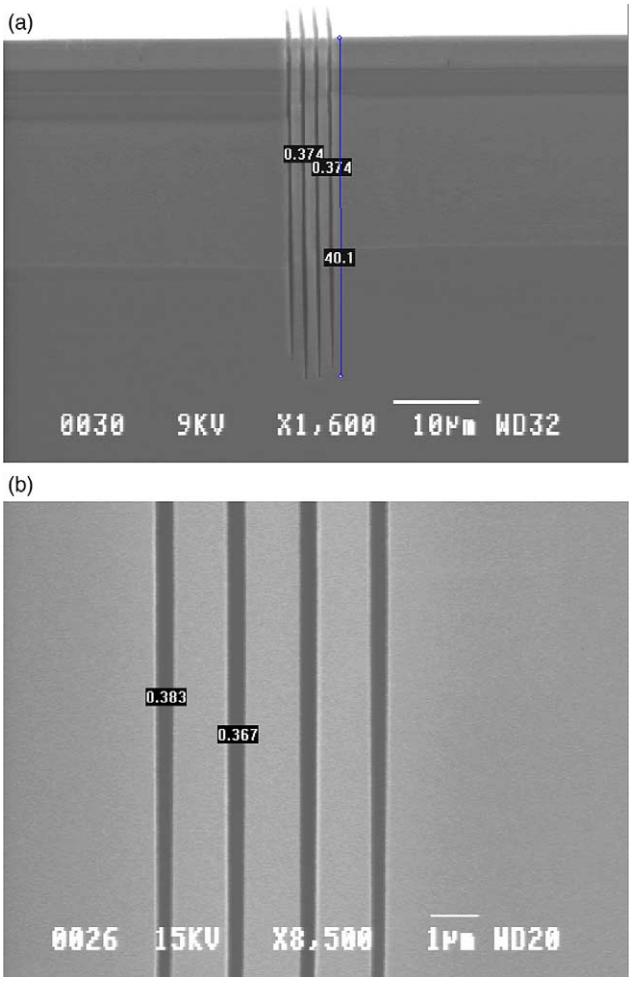

Fig. 1. (a) Silicon sub-micron deep trenches obtained by DRIE. Evidence is given of 0.374 μm—wide, 40.1 μm—deep trenches, corresponding to an aspect ratio of 107, (b) detailed view.

and holes as well as silicon walls and pillars having sub-micron feature sizes.

All our DRIE experiments were performed on an ALCATEL 601E System. Fig. 1 shows our latest results related to deep etching of sub-micron trenches. One can see 0.374 μm—wide, 40.1 μm—deep trenches, corresponding to an aspect ratio of 107. To our knowledge, this value of the aspect ratio is at the moment the highest ever obtained using a DRIE process.

The high aspect ratio micro- and nanostructures under consideration are obtained from three main process steps. First electron-beam (EB) lithography is performed in order to pattern nanostructures on an aluminum thin film layer, having a thickness of typically 200 nm. Then aluminum is etched using a chlorine-based chemistry in a conventional reactive ion etching (RIE) system. The third step consists of silicon deep etching with aluminum as a hard mask.

An ICP-RIE plasma etcher (Alcatel 601E) is used for this purpose. This equipment is configured with an ICP Radio Frequency source of 2 kW and a low frequency generator, for wafer polarization. Wafer is clamped with a mechanical chuck. In the experiments presented in this paper, the wafers were maintained at a temperature of 20 °C.

HARMS with openings in the range of 0.3–1 μm are obtained by tuning key parameters such as pressure, bias voltage and gas switching (SF_6/$C4F_8$). In order to achieve important depth, strong ion bombardment is needed. This ion bombardment also drastically affects the mask/Si selectivity. Therefore, photoresist or other soft mask materials cannot be used for this kind of experiments. Moreover, etching time for a sub-micron feature size is quite long due to ARDE effect. Typical etching rates are below 1 μm/min. Using a 200 nm-thick aluminum mask, the bias voltage is adjusted to maximize ion bombardment without reaching the limit value that induce mask sputtering. The pressure is also maintained to a low value between 2 and 2.5 Pa.

It is noteworthy that the developed process is specific to patterns of small dimensions only. Black silicon and excess of passivation appears on patterns with dimensions larger than 10 μm. Therefore, when a design requires the simultaneous fabrication of small openings (sub-micron) and large openings (10 μm and above), a two-mask approach should be used, in which etching of small features is separated from etching of large features.

2.2. Application of sub-micron HARMS to photonics

At the sub-micron scale, the roughness due to the scalloping introduced by the alternating (etching/passivation) steps of the Bosch process can be non-negligible. To minimize this effect, we set the switching time to a lower value than in conventional processes. The resulting peak-to-valley roughness can be reduced to 20 nm. Cryogenic process, which is expected to be more efficient in terms of surface quality of the sidewalls, was also studied as an alternative to optimized Bosch process. Examples of etching results using the cryogenic process are shown in Fig. 2.

The above-mentioned recent advances in the fabrication of sub-micron HARMS with high AR opens the way to new applications in photonics.

Among these applications to photonics one can mention the vertical distributed Bragg reflectors (DBRs) [4,5], which consist of alternating vertical silicon thin walls separated by thin air-gaps. Silicon and air are two materials with high index contrast (used namely in photonic crystals). These DBR's with vertical architecture form mirrors of high reflectivity with an optical axis in the plane of the substrate. Therefore, high quality, horizontal, Fabry–Pérot cavities are attainable. Moreover, association of these optical components with MEMS actuators is also possible using Silicon on insulator (SOI) substrates and it leads to new functionalities such as tunability and reconfigurability. An illustration of this is the tunable optical filter [5] shown in Fig. 3. It is noteworthy that the sub-micron HARMS with high AR also opens very promising application to devices based on photonic crystals.

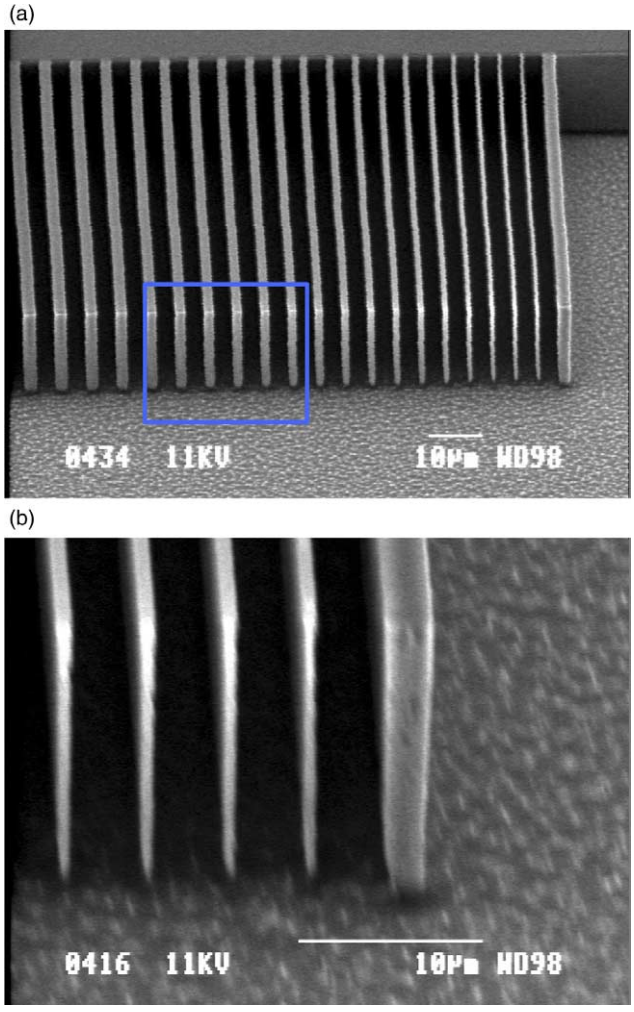

Fig. 2. (a) Silicon walls. Width ranging from 0.3 to 3 μm and depth of 15 μm, obtained with a cryogenic process, (b) detailed view.

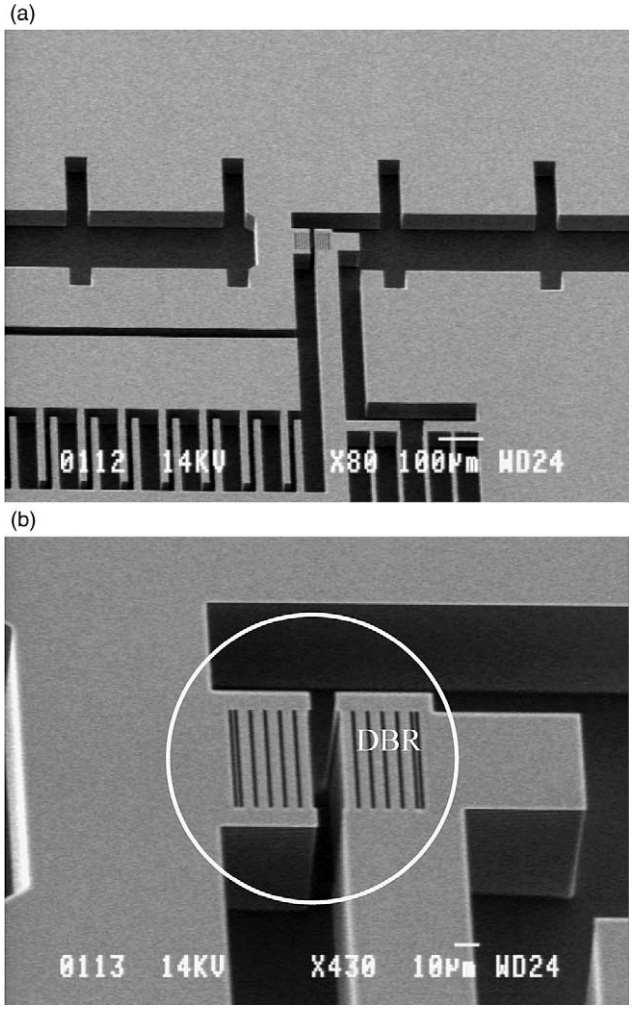

Fig. 3. (a) Tunable optical filter consisting of two freestanding vertical DBR mirrors. The air gap distance between the two mirrors is controllable using integrated electrostatic actuators. DRIE performed on SOI wafer. Detailed view.

3. Isotropic processes

3.1. Using ICP reactor in isotropic conditions for 3D micromachining

In almost all cases, the main goal of using DRIE is the realization of vertical and deep HARMS. We also used the ALCATEL ICP reactor in isotropic conditions (using SF_6 chemistry) in order to test the MEMSNAS process, which was proposed as a new 3D micromachining technique [7]. MEMSNAS is an acronym for Micro-loading Effect for Micromachining 3D Structures of Nearly All Shapes. Nearly all shapes are indeed obtainable by this process by taking advantage of the microloading effect: an array of holes of different diameters is first made on a hard mask, which is typically an aluminum thin film. Then isotropic etching is performed. The result of this etching is an array of overlapping (quasi-) hemispheres having different diameters according to the microloading phenomenon. The hard mask is then removed and finally a second isotropic etching is performed to smooth the surface. The final result is the envelope of the 3D shape designed through the hole diameters distribution. For the MEMSNAS process, the main benefit of using the ICP reactor is the higher speed than that obtained with conventional RIE systems, which is mainly due to the higher plasma density. An example of the resulting silicon 3D structures is shown in Fig. 4. Furthermore, such 3D structures were used as a mold for the fabrication of 3D devices in Poly di-Methyl-Siloxane (PDMS). In addition to the applications in microoptics, this new technology is very promising for microfluidic applications as well.

3.2. Combination of anisotropic and isotropic process

The isotropic process mentioned above was combined with the anisotropic (Bosch) process in order to obtain new shapes, unattainable with the above-mentioned techniques.

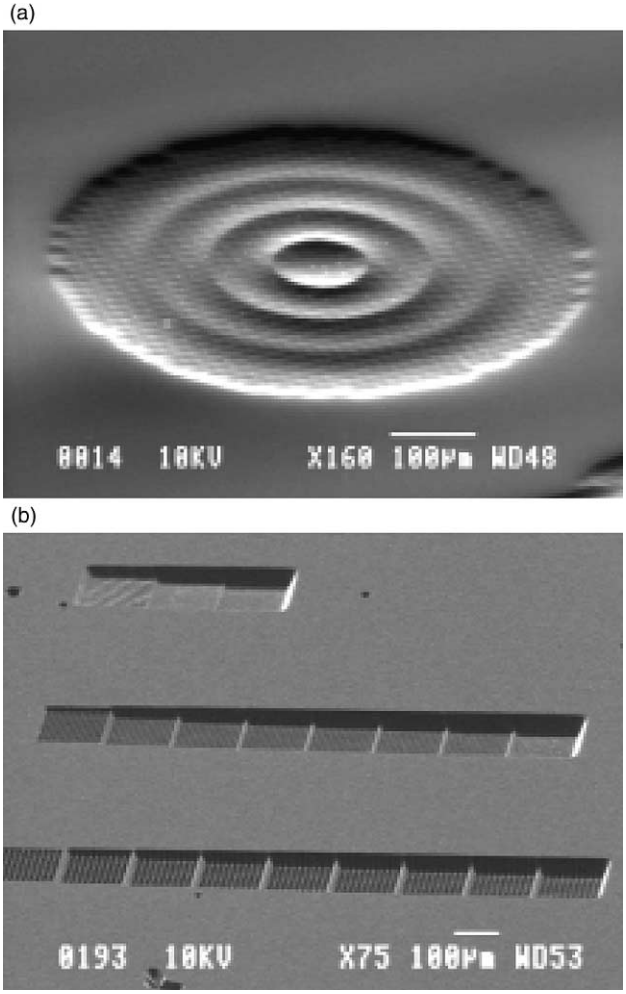

Fig. 4. 3D silicon structure obtained on a DRIE system using the MEMSNAS process. (a) Fresnel lens, (b) staircase structure for process calibration.

An illustration of such a combination is shown in Fig. 5. It consists of alternating a few periods of Bosch process (leading to straight sidewalls) and isotropic etching. Such structures have applications both in photonics (3D photonic crystals and buried all-silicon waveguides) and in microfluidics (micromixers, filters and buried microchannels [8] that can be multiple and at different depths).

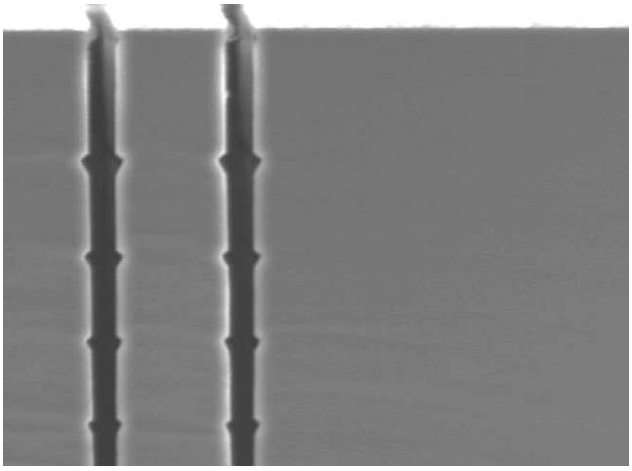

Fig. 5. Combination of anisotropic and isotropic etching.

Another non-conventional use of DRIE is the combination of isotropic and anisotropic etching to achieve a Single Crystal Reactive Etching and Metallization SCREAM-like process [9], which provides a way to realize freestanding single-crystalline silicon microstructures without the need for SOI wafers. In this new process, the passivation by thermal oxide, which is used in the original SCREAM process, is replaced by an in situ passivation

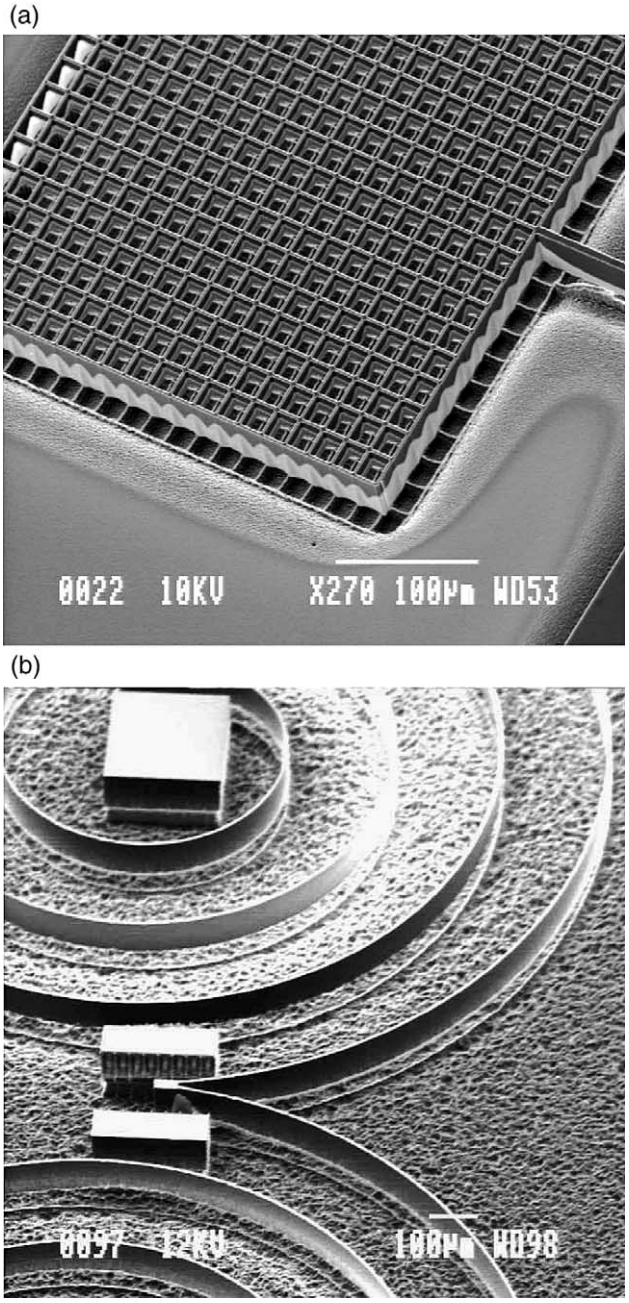

Fig. 6. Freestanding, single crystalline silicon microstructures obtained by a SCREAM-like process, all steps after patterning being performed in the same equipment, an ICP reactor.

step, in the ICP reactor. A summary of the process is the following: (i) deep etching using Bosch process; (ii) reinforcement of sidewall passivation using C_4F_8 chemistry; (iii) anisotropic etching using SF_6 chemistry and finally; and (iv) isotropic etching using SF_6 chemistry for the microstructure release. Contrary to the original SCREAM process, all steps after patterning are performed here using the same equipment, an ICP reactor. Fig. 6 shows examples of MEMS devices, which result from this process. One can see in Fig. 6(a) a released silicon structure with the remaining sidewall passivation layer, which appears in light gray on the picture.

On the other hand, it was shown recently by Sarajlic et al. [10] that this process can be improved to allow the manufacturing of electrically isolated, freestanding silicon microstructures on standard silicon wafers, that is, without the need for SOI wafers as well.

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